THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 47

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YOHJI WATANABE
and KENJI TSUCHIDA

Appeal No. 1997-2383
Application 08/150,782

ON BRIEF

Before URYNOWICZ, HAIRSTON and LALL, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 3-6 and 8-16.

The disclosed invention relates to a dynamic random access memory device that transitions to an intermediate potential level between a power source voltage level and a

ground voltage in response to an address transition detection signal.

Claim 5 is illustrative of the claimed invention, and it reads as follows:

5. A dynamic random access memory comprising:

an array of rows and columns of memory cells;

parallel word lines associated with the rows of said memory cells;

parallel bit lines transverse to said word lines and associated with the columns of said memory cells;

a sense amplifier coupled to said array of memory cells to read out data directly from said memory cells;

row decoder means, coupled to said word lines, for receiving a row address signal, and for selecting a corresponding one of said word lines;

column decoder means, coupled to said bit lines and said sense amplifier, for receiving a column address signal to select a corresponding one of said bit lines;

first data lines coupled to said bit lines by transfer gates which are selectively controlled by said column decoder means whereby readout data output from said sense amplifier is transferred to said first data lines;

a data input/output buffer coupled to said first data lines and including a CMOS current mirror differential amplifier activated in a ready mode to amplify the readout data on said first data lines;

second data lines connected to said first data lines through said data input/output buffer and passing data amplified by said differential amplifier thereof;

address transition detecting means for detecting transition of the row and column address signals, and for generating an address transition detection signal;

equalizing means, coupled to said second data lines and said address transition detecting means, for resetting said second data lines, to which the amplified data from said differential amplifier is supplied, at a preselected potential level, said equalizing means including switching means for connecting said second data lines to said preselected potential level in response to the address transition detection signal, said preselected potential level being an intermediate potential between a power source voltage and a ground voltage of said memory; and

data latch means connected to said differential amplifier through said second data lines for latching the amplified data.

The references[1] relied on by the examiner are:

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[1]The following references are cited for their teachings of an intermediate voltage (i.e., 1/2 Vcc):

Watanabe et al. (Watanabe) 4,967,395 Oct. 30, 1990

Tsuchida et al. (Tsuchida), "The Stabilized Reference-Line (SRL) Technique for Scaled DRAM's," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pages 24-29 (Feb. 1990).

Shinoda	4,811,295	Mar. 7, 1989
Nakano et al. (Nakano)	4,870,617	Sept. 26, 1989
Hayakawa et al. (Hayakawa)	4,922,461	May 1, 1990

Minato et al. (Minato), "Session XV: Static RAMs. IEEE International Solid-State Circuits Conference," pages 222-23 (1984).

Claims 3-6 and 8-16 stand finally rejected under 35 U.S.C. §103(a)as being unpatentable over Shinoda in view of Hayakawa or Minato, each taken separately, further in view of Nakano.

Reference is made to the briefs and the answer for the respective positions of the appellants and the examiner.

OPINION

The obviousness rejection of claims 3-6 and 8-16 is reversed.

According to the examiner (Answer, page 4), Shinoda discloses (Figs. 1-2 and column 6, lines 23-46) all of the means and steps of claims 3-6 and 8-16, except for a teaching of the "address transition means" and the 1/2 Vcc precharge potential level of the second data lines. The examiner concludes (Answer, page 6) that it would have been obvious to apply the teachings of Hayakawa or Minato to Shinoda to improve the data read out operation because the secondary references disclose high speed operation through the use of address transition detection. The examiner is also of the opinion (Answer, pages 6 and 7) that it would have been obvious to the skilled artisan "to equalize the data bus lines of Shinoda as taught by Nakano to an intermediate potential level between Vcc and ground in order to reduce noise and decrease the time it takes the sense amplifier to bring the data bus lines to their full complementary logic levels."

Appellants argue (Brief, page 5) that Shinoda does not teach the "address transition detecting means," the "precharge potential level of the second data lines" or the particular "equalization circuits" of the claimed invention. Appellants also argue (Brief, page 6) that Hayakawa discloses a SRAM which cannot use a 1/2 Vcc pre-charge scheme, and that Hayakawa does not disclose an intermediate potential between Vcc and ground for equalizing the second data lines, the I/O output differential amplifier, or the "equalization means." With respect to Nakano, Appellants argue (Brief, page 8) that Nakano discloses equalizing transistors in a DRAM, but "does not teach the provision of CMOS differential amplifiers arranged at the front stage of a latch circuit, with an intermediate potential between a power source voltage and a ground voltage of the memory being equalized on the claimed 'second data lines' at the input to the data latch circuit." Lastly, Appellants argue (Reply Brief, page 1) that the combining of the references is based on hindsight speculation. We agree. Hayakawa is completely silent concerning the use of a DRAM, wherein the address transition means is arranged to cause an intermediate potential between Vcc and ground for

equalizing the second data lines. The same holds true for Minato. Nakano discloses 1/2 Vcc in a DRAM, but such potential level is not reset as a result of an address transition detection signal as claimed.

In summary, the obviousness rejection of record cannot stand.

DECISION

The decision of the examiner rejecting claims 3-6 and 8-16 under 35 U.S.C. § 103(a) is reversed.

REVERSED

STANLEY M. URYNOWICZ, JR. Administrative Patent Judge	)
KENNETH W. HAIRSTON Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)

KWH:hh

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